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Next-generation Packaging Requirements

Semiconductor packaging has a significant impact on the overall device performance. Traditional packaging technologies are reaching their limits in terms of the performance, size and scalability required to meet the needs of emerging applications. Current and future demands of microelectronic systems in terms of performance, power consumption and reliability at a required cost are met by developing advanced silicon process technology, innovative packaging solutions based on chip and package system co-design, low cost materials, reliable interconnect technologies, and advanced assembly and test.

For internet connected devices, there are four interrelated requirements for an effective packaging solution: 1) Cost effectiveness, 2) Thinner and smaller form factor, 3) High performance, and 4) Integration. For mobile, IoT and WE devices, three types of integrated circuits (ICs) will be the primary drivers of semiconductor growth: 1) Specialized low-power microcontrollers (MCUs, embedded processors with non-volatile memory (NVM) and power management functions); 2) Connectivity (Wi-Fi, Bluetooth®, GPS, cellular, ZigBee®, etc.); 3) Sensors and actuators (MEMS, image sensors, others).

These applications listed above and ICs require different process technology nodes and different process technologies—MCU (digital + mixed-signal + non-volatile memory), connectivity (RF + analog + antenna/security) and sensors (MEMS and non-MEMS). System-on-chip (SoC) could be an attractive solution if different functions can be placed in the same wafer fab solution. However, achieving such an all-in-one SoC solution can be quite difficult and often very costly. An alternative approach is to balance silicon-level and package-level integration, as evidenced by rapid expansion of system-in-package (SiP) modules. SiP modules provide the ability to not only integrate multiple technologies, but also additional components such as passives, antennas, etc., to create fully functional sub-systems. To illustrate the potential for miniaturization by use of SiP modules, Xiaomi's low-cost, high- performance MI3 smartphone, for example, contained approximately 850 electronic components, including ~22 filters, ceramic crystals, oscillators, ~103 diodes and small transistors, and ~670 passives.

Advanced Wafer-Level Technology ; eWLB/FO-WLP

As a small, lightweight, high performance semiconductor package, wafer-level chip-scale packaging (WLCSP) has been a popular solution for space constrained mobile devices and is a compelling solution for new IoT and WE applications. WLCSP was introduced in the late 1990s as a semiconductor package wherein all manufacturing operations are performed in wafer form with dielectrics, thin-film metals and solder bumps applied directly on the surface of the die with no additional packaging [2]. The WLCSP provides the smallest possible package size since—the final package is no larger than the die itself. The volume of WLCSP used in the industry has experienced steady growth – driven by the small form

silicon (Si) nodes, eWLB solutions are in high-volume production on 28nm and starting to ramp on 20nm devices.

eWLB products found in various mobile products and consumer electronics

There are a number of cases where eWLB has helped semiconductor companies achieve very specific and measureable results. Following are some examples as shown in Figure 3:

PoP bottom has 300um package height so total stacked PoP height could be less than 0.8 mm after top memory package stacking (body thickness of 0.45mm). Table 1 shows value proposition of 3D eWLB-PoP technology.

(a) (b)

(c) (d)

(e)

WLPs, such as low assembly cost, minimum dimensions and height, as well as excellent electrical and thermal